Reliable Control of Filament Formation in Resistive Memories by Self-Assembled Nanoinsulators Derived from a Block Copolymer

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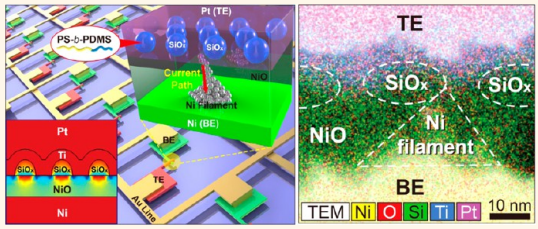
ABSTRACT Resistive random access memory (ReRAM) is a promising candidate for future nonvolatile memories. Resistive switching in a metal—insulator—metal structure is generally assumed to be caused by the formation/rupture of nanoscale conductive filaments (CFs) under an applied electric field. The critical issue of ReRAM for practical memory applications, however, is insufficient repeatability of the operating voltage and resistance ratio. Here, we present an innovative approach to reliably and reproducibly control the CF growth in unipolar NiO resistive memory by exploiting uniform formation of insulating SiO_x nanostructures from the self-assembly of a Si-containing block copolymer. In this way, the standard deviation (SD) of set and reset voltages was markedly reduced by 76.9% and 59.4%, respectively. The SD of high resistance state also decreased significantly, from 6.3×10^7 Ω to 5.4×10^4 Ω. Moreover, we report direct observations of localized metallic Ni CF formation and their controllable growth using electron microscopy and discuss electrothermal simulation results based on the finite element method supporting our analysis results.



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Resistive random access memory (ReRAM), which shows two or more stable resistance states through electrical stimuli, has strong potential to be one of the next generation nonvolatile memories (NVM). It is expected that charge-based memories such as dynamic random access memory (DRAM) and flash memory potentially can be replaced by ReRAM owing to its fast write/erase speed, low power consumption, simple structure, and extreme scalability.[1−7] ReRAM is divided into two different categories depending on switching behaviors, unipolar and bipolar switching modes.[3] Unipolar switching does not depend on the polarity of the voltage signal (reset/set), whereas bipolar switching takes place for different polarities. Notably, unipolar switching behaviors are closely related to the formation and rupture of conductive filaments (CFs), mainly caused by oxygen vacancy migration resulting from local redox processes and thermal effects.[8] Several groups recently reported direct observation of nanoscale CFs using *ex-situ* and *in situ* transmission electron microscopy (TEM) in resistive switching oxides such as TiO_2, SiO_2, ZnO, and ZrO_2.[4,9−11] Unipolar resistive memories based on NiO, CuO, ZnO, and SiO_2 have a number of advantages such as high scalability, good reliability, and a large R_{on}/R_{off} ratio.[10,12−16] Its key concern for NVM applications, however, is large fluctuations of switching voltages and resistances caused by random growth/rupture of CFs.[5,8,17−20] This would also result in serious problems for multilevel cell (MLC) storage, which is required for further increases of data storage density. In efforts to resolve the problem of irregular formation of CFs, previous studies have suggested various solutions including optimization of the crystallographic structure,[21] incorporation of an interfacial layer,[18,19] doping of

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impurities,[22] and insertion of metal nanoparticles.[17] Nevertheless, sufficient device performance enhancement together with clear evidence of a corresponding switching mechanism has not been presented yet.

In this work, uniformly distributed SiO_x nanodots (SiO_x-NDs) generated by the self-assembly of Si-containing poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) block copolymers (BCPs) were incorporated at the interface between a resistive switching (RS) material (NiO) and a top electrode (Pt/Ti) to control the locations where the CFs were formed. The self-assembly of BCPs has attracted considerable attention during the past few decades because it can generate sub-20 nm periodic patterns with various morphologies such as dots, lines, holes, and rings as a result of a microphase separation of the mutually incompatible polymer blocks.[23−25] Self-assembled nanostructures are currently providing useful and practical applications in many fields because of their excellent resolution, process simplicity, and compatibility with conventional complementary metal-oxide semiconductor (transistor type) processes.[14,26,27] The excellent cost-effectiveness and reliability of directed self-assembly (DSA) based on BCPs have stimulated semiconductor industries to achieve the practical combination of traditional ArF lithography with DSA and its implementation on 300 mm wafers,[28−32] suggesting it as a strong candidate for sub-10 nm resolution enhancement technology. Especially in the case of PS-*b*-PDMS BCPs, the self-assembled PDMS microdomains in the PS matrix can readily be transformed into thermally stable and insulating SiO_x nanostructures after a short O_2 plasma treatment.[14,24−26,33] The self-assembled SiO_x-NDs in unipolar NiO resistive memories can extensively modify both the electric field and temperature distributions, as will be shown in our simulation results. Our BCP-engineering methodology can induce highly selective, controlled formations of CFs inside NiO thin films. Variations of operating voltages and resistance ratios can thereby be significantly reduced. In this study, we not only demonstrate the formation/rupture of filaments in NiO resistive memory but also provide the microscopic mechanisms of performance enhancement using high-resolution transmission electron microscopy (HRTEM) analysis and energy dispersive spectrometer (EDS) elemental mapping results. In addition, electro-thermal simulation results theoretically support the selectively controlled formation of metal filaments inside NiO thin films.

RESULTS AND DISCUSSION

Structure of Resistive Memory Devices. Our device structure consists of a top electrode (TE), self-assembled SiO_x-NDs, RS material, and a bottom electrode (BE), as schematically illustrated in Figure 1a. Both the BE (Ni/Cr) (250 nm/20 nm) and the TE (Pt/Ti) (250 nm/10 nm) were deposited by radio frequency (RF) sputtering on a SiO_2/Si substrate. The RS material (NiO, 20 nm) was formed on the Ni films by reactive ion etching (RIE) plasma oxidation with O_2 gas, resulting in amorphous NiO films due to the high bombarding energy of the ionic species and the low temperature (room temperature), as shown in Supporting Information Figure S1, whereas NiO films deposited by sputtering or atomic layer deposition (ALD) were usually polycrystalline.[18,19,34,35] For the formation of SiO_x-NDs, a sphere-forming PS-*b*-PDMS BCP (MW = 56.1 kg/mol, f_{PDMS} = 17.1%) was spin-casted on PS-OH (MW = 22 kg/mol) brush-coated NiO films, annealed under toluene vapor for the promotion of self-assembly at room temperature, and treated with CF_4 and O_2 plasma to convert the PDMS spheres into SiO_x-NDs. During the process of O_2 plasma treatment, the PS layer on the NiO films was completely removed *via* sufficient plasma oxidation. The structures of the reference samples were identical except for the absence of SiO_x-NDs. More details of the device fabrication process are provided in Figure S2. Figure 1b shows an optical image of a 16 × 16 cell array whose unit cell has a 10 × 10 μm^2 cross-point structure. The uniform formation of self-assembled 20 nm-diameter SiO_x-NDs between the TE (Pt/Ti) and the active layer (NiO) was confirmed by SEM, TEM, and EDS elemental mapping analyses (Figure 1c and Figures S3 and S4).

Electrical Performance Evaluations. To evaluate and compare the performances of the devices, direct current (DC) voltage sweeping was applied to the TE (Pt/Ti), while the BE (Ni) was grounded. Before repeating the voltage sweeping, electroforming of the devices was performed under a compliance current (CC) of 1 mA (Figure S6). The voltages for the forming process of a cell with SiO_x-NDs (2.4−3.3 V) tended to be lower than those for a conventional cell (without SiO_x-NDs) (5.9−7.3 V). This implies that, in the case of the SiO_x-NDs device, electric fields perpendicular to the device are concentrated on the locations between SiO_x-NDs, facilitating the initial formation of CFs and consequently resulting in a reduction of the forming voltage. This lower electroforming voltage, enabled by controllable and selective CF formation, is beneficial because high forming voltage is a severe obstacle for scaling the circuit design.[36] The initial resistance tended to decrease with an increase in the device area for both the conventional device and SiO_x-NDs devices. The initial resistance of the SiO_x-NDs devices was larger than that of the conventional devices because of the reduction of the contact area between NiO and the TE. After the electroforming process, both devices showed typical unipolar switching behavior, that is, the same reset/set switching polarity. Current−voltage (*I*−*V*) curves for the first 50 cycles are shown in Figure 2a (conventional device) and Figure 2b (BCP self-assembled SiO_x-NDs device). Also, the operating voltage distributions during 100 cycles for each cell are

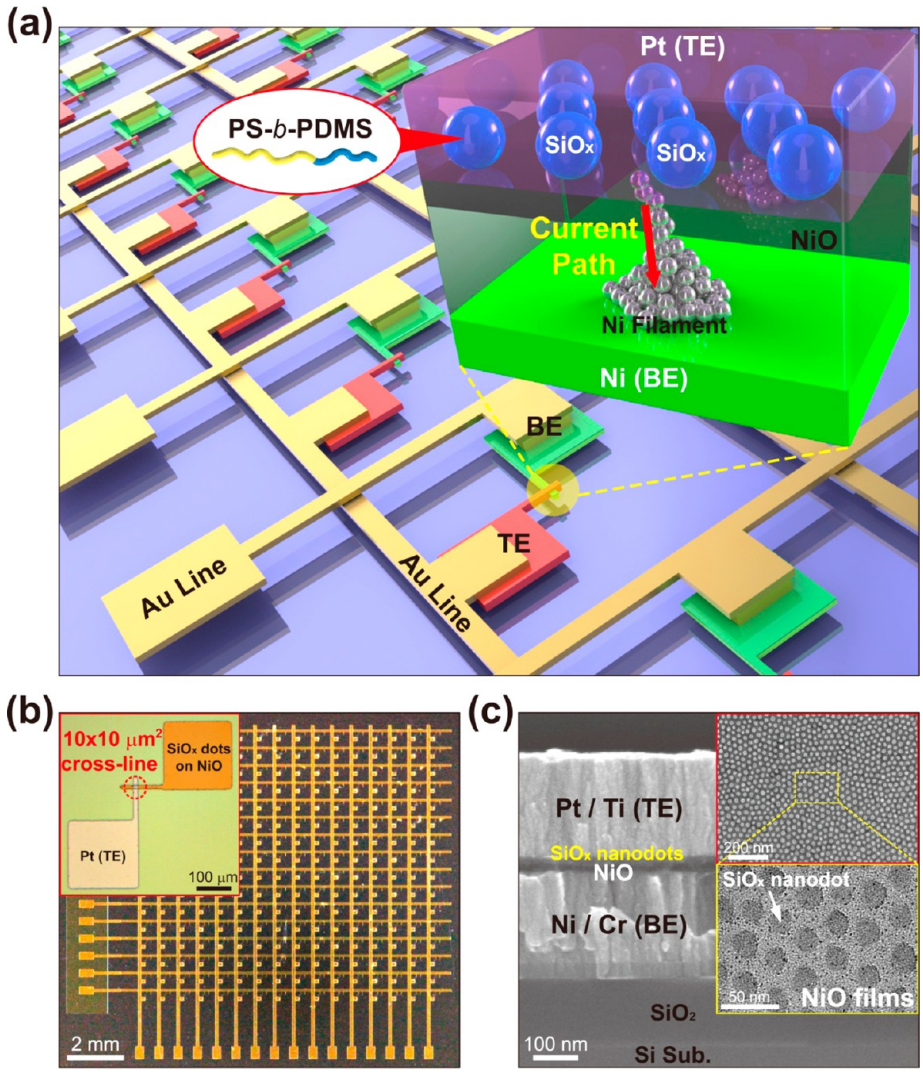

Figure 1. Device structure of the NiO resistive memory inserting self-assembled SiO_x nanostructures. (a) Schematic of NiO memory with SiO_x-NDs and its operating mechanism through Ni CFs. The TE, active layer, and BE are Pt, NiO, and Ni, respectively. Self-assembled SiO_x-NDs are formed by solvent annealing and plasma etching of Si-containing PS-*b*-PDMS block copolymers. (b) Optical image of a 16 × 16 cell array for NiO resistive memories. The inset shows the unit cell of memories with 10 × 10 μm^2 cell area. (c) Cross-sectional SEM image of NiO resistive memory with SiO_x-NDs. The insets are SEM and TEM top-view images of hexagonally formed SiO_x-NDs on NiO films before TE (Pt/Ti) deposition.

presented as histograms and statistical charts in Figure 2 panels c and d, revealing that the repeatability of the cell with the SiO_x-NDs was drastically improved and that the variation of the set/reset voltages was much narrower than that of the conventional cell. The reset and set operating voltage ranges of the conventional cell were 0.5−1.84 V and 1.01−4.61 V, and those of the cell with SiO_x-NDs were 0.54−0.99 V and 1.33−2.0 V, respectively. For the conventional device, the average values of set/reset voltages were 2.3 V/0.89 V, and the standard deviations (SD) of set/reset voltages were 0.79 V/0.25 V, respectively. Conversely, for the SiO_x-NDs device, the average values of set/reset voltages were 1.6 V/0.77 V, and the SD of set/reset voltages were 0.18 V/0.10 V, respectively. Here, we used SD as a quantitative measure of data variation. The SD of set and reset voltages was markedly reduced by 76.9% and 59.4%, respectively, through the incorporation of SiO_x-NDs. For the SiO_x-NDs cell, the decrease of the set voltage (V_{set}) variation was more remarkable than the reset voltage (V_{reset}) variation because the insulating SiO_x-NDs resulted in a concentration of electric fields on the NiO top surface that was not covered by the nanodots; this enabled selective and controlled growth of CFs. In addition to the V_{set} variation for the SiO_x-NDs cell, the uniformity of V_{reset} was also improved significantly. The heat generated by Joule heating can be concentrated around the filament region because the SiO_x-NDs play a role as nanoscale thermal insulator due to its low thermal conductivity. The low thermal conductivity of the SiO_x-NDs can maintain the constant energy to rupture the filament during the repeated reset process; thus, the distribution of V_{reset} decreased. This mechanism is well

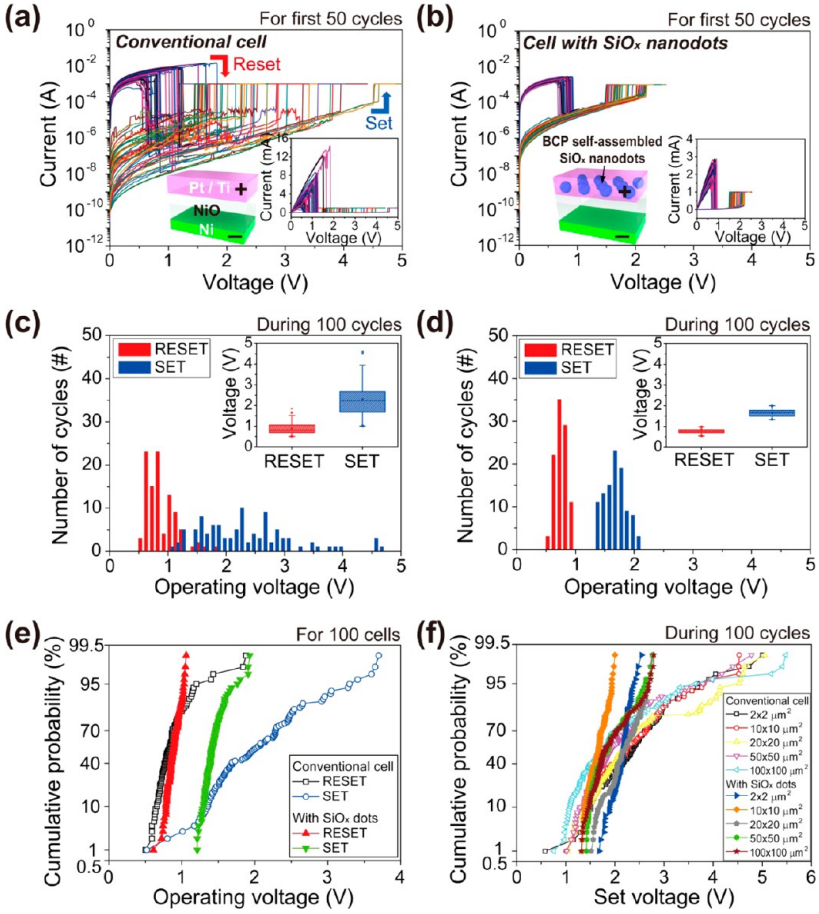

Figure 2. Operating voltage distributions of NiO resistive memory devices without/with self-assembled SiO_x-NDs. $I-V$ curves in semilogarithmic scale from the NiO memory devices during the first 50 cycles (a) without SiO_x-NDs (conventional cell) and (b) with self-assembled SiO_x-NDs. The inset shows their $I-V$ curves in linear scale. The current compliance for the set operations is 1 mA. Histograms of the reset/set operating voltage in each unit cell (c) without and (d) with SiO_x-NDs during 100 cycles. The insets show operating voltage statistical charts from the unit memory cell without/with SiO_x-NDs. Cumulative probability graphs of operating voltage (e) in 100 memory cells and (f) in various cross-line electrode areas (2×2, 10×10, 20×20, 50×50, and 100×100 μm^2) without/with SiO_x-NDs.

substantiated by our electro-thermal simulation shown in Figure 5d. In contrast, for the conventional cell, the wide heat spread out to the surrounding area of the filament as shown in Supporting Information, Figure S19b. In addition to increasing V_{set}/V_{reset} reproducibility, the programming voltage margin ($V_{set,\,min} - V_{reset,\,max}$) of the SiO_x-NDs device was 0.34 V (1.33−0.99 V), achieving improved reliability during memory operations. On the other hand, the reset/set voltage overlap of the conventional cell was large, which might cause programming error. The cell-to-cell variations of V_{set} and V_{reset} were also investigated from the 100 different cells of the 16×16 cell array interconnected with gold electrodes, as shown in Figure 1b. The cell-to-cell uniformity in the SiO_x-NDs device was markedly superior, as shown in the cumulative probability graphs of Figure 2e.

It is evident from Figure 2 panels a−e that the locally formed SiO_x-NDs can improve the uniformity of the operating voltage in the resistive memory cell of $10 \times 10\,\mu m^2$. Thus, in order to identify the scalability of this approach, it is necessary to confirm whether the same trend occurs in the devices with different electrode areas. NiO unipolar memories with various electrode areas such as 2×2, 10×10, 20×20, 50×50, and $100 \times 100\,\mu m^2$ were fabricated and characterized. The electroforming data and optical images of these devices are shown in Supporting Information, Figures S6 and S7, and the $I-V$ curves and the operating voltage distributions of devices without/with SiO_x-NDs depending on the electrode areas are shown in Figure S8. The V_{set} and V_{reset} variations in all the cells with various electrode areas decreased in the same manner (Figure 2f and Figure S9a). Here, it should be noted that the effect of SiO_x-NDs tended to increase for the smaller electrodes (Figure S10b). We believe that the filament formation process is more reproducible for smaller electrodes, caused by the rapid decrease of filament formation spots in the SiO_x-NDs cell with reduction of the electrode area. On the other hand, for the conventional device, there is no dependence on electrode area although the area for filament growth

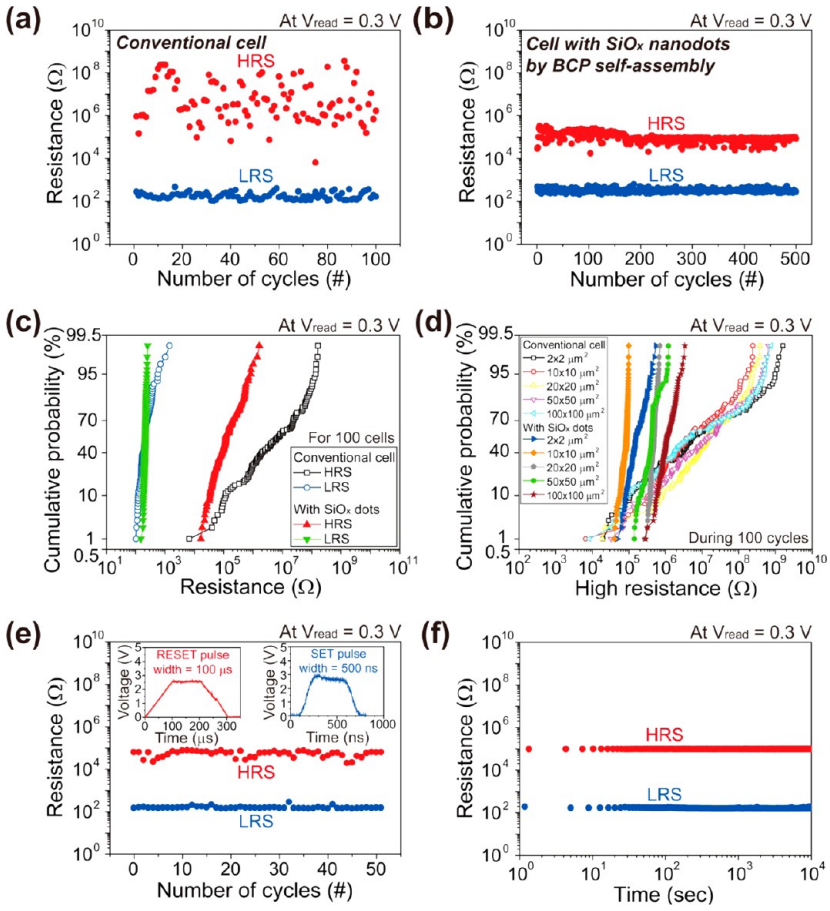

Figure 3. Device reliability evaluations and resistance states distributions in NiO resistive memories without/with SiO_x-NDs. Write endurance results by DC sweeping mode in (a) the conventional cell and (b) the cell employing SiO_x-NDs. Cumulative probability graphs of resistance states (c) in 100 cells and (d) in various electrode areas without/with SiO_x-NDs. (e) Endurance performance of NiO memory cell ($10 \times 10\ \mu m^2$) with SiO_x-NDs by using a reset pulse (100 μs) and a set pulse (500 ns). (f) Retention measurement of NiO memory cell ($10 \times 10\ \mu m^2$) with SiO_x-NDs. The read voltage for all resistance measurements is 0.3 V.

decreased by 2500 times (Figure S10a). In our device size, nanoscale CFs are much smaller than the electrode areas, resulting in the random filament growth/rupture. If the device size shrinks to the sub-100 nm, the RS uniformity will be improved with the further decrease of device area. An additional interesting point was that the uniformity improvement by SiO_x-NDs was substantial regardless of the cell size. The average diameter and distance between SiO_x-NDs (20 and 15 nm, respectively) were much smaller than the electrode areas (4 μm^2–10000 μm^2). This indicates that the CFs inside NiO materials are locally formed at the nanoscale,[17,19,21,34,35,37] and thus the self-assembled SiO_x-NDs can effectively control the CFs of NiO unipolar memory.

Figure 3 panels a and b show the write endurance of the conventional cell and the BCP self-assembled SiO_x-NDs cell, respectively. The cell size was fixed at $10 \times 10\ \mu m^2$. Their reset/set switching characteristics were measured using the DC sweep mode and a reading voltage of 0.3 V. For the conventional cell, the high resistance state (HRS) in particular showed very large variation between about 10^5 to 10^9 Ω. In general, the HRS/LRS fluctuation can be attributed to the stochastic nature of the oxygen vacancy diffusion processes, leading to LRS resistance variation originating from the number and/or the size of the CFs and the HRS resistance variation resulting from the length distributions of ruptured filaments, because the tunneling current is highly dependent on the tunneling gap distance.[8] It is thus necessary to reproducibly control the repeated growth and rupture of filaments in the active switching area for reduction of the resistance variation. In contrast, the R_{on}/R_{off} ratio of the cell with SiO_x-NDs was highly stable during the repeated 500 cycles. We presented the further cycling endurance test for the device with SiO_x-NDs, suggesting the reliable RS operation. The average value and the SD of HRS resistance were 3.2×10^7 Ω and 6.3×10^7 Ω for the conventional device, and were 1.1×10^5 Ω and 5.4×10^4 Ω for the SiO_x-NDs device, respectively; therefore, the SD of HRS resistance decreased significantly, from 6.3×10^7 Ω to 5.4×10^4 Ω. The uniformity improvement of reset voltage/current

induced the reduction of the length distribution of the ruptured filaments, leading to the uniform HRS resistance. The R_{on}/R_{off} ratio decreased from about 10^2-10^6 Ω to 10^2-10^3 Ω by the incorporation of SiO_x-NDs into the device as shown in Figure 3a,b. The HRS resistance is determined by the length of the ruptured filaments, and thus a high HRS resistance is induced by a shorter length of ruptured filament. For the conventional device, the large variation of HRS resistance is caused by the unpredictable reset switching behavior, causing highly dispersive lengths of ruptured filaments (Figure S11 in the Supporting Information). The nonuniform heat generation from randomly formed filaments can result in temperature variation due to thermal interference and consequently the HRS resistance. On the other hand, the incorporation of insulating SiO_x-NDs can reduce the thermal interference due to the more homogeneous formation of filaments. This can reduce the length distribution of the ruptured filaments after reset operation, leading to more uniform HRS resistance successfully by eliminating the high HRS resistance values (Figure 5d). Therefore, we achieved stability and repeatability of resistance states during the writing endurance test, removing the unpredictable high HRS resistance. The R_{on}/R_{off} ratio of 10^2-10^3 Ω to the memory window was also enough for applications to the ReRAM.[5]

The cell-to-cell distribution of HRS/LRS for 100 different cells was also improved, as shown in Figure 3c. Even though the conventional cells have a very large resistance fluctuation with 4 orders of magnitude, we believe that the improvement by 2 orders of magnitude is very significant. Furthermore, the variations of HRS/LRS upon 100 cycles were reduced in the case of the SiO_x-NDs cells for all the electrode areas (Figure 3d and Figure S9b). As mentioned above, the improvement of the resistance fluctuation is related to the position-specific growth/rupture guided by the localized SiO_x-NDs. The relationship between the LRS resistance and device area was such that the LRS resistance decreased with an increase in the electrode area (Figure S9b in the Supporting Information). The resistance state was dependent on the device area, once the CFs were connected to the TE during the initial electroforming process. It is obvious that the resistance is inversely proportional to the electrode area. However, in the case of the HRS, the resistance state was more dependent on the length of ruptured filaments than the device area, as shown in Figure S11. From these results, we can conclude that the embedding of SiO_x-NDs in the NiO memory device can improve not only the operating voltage variations but also the resistance ratio variations.

A pulse switching test was also implemented for the memory cells containing SiO_x-NDs. Pulses with 2.5 V/100 μs and 3 V/500 ns were applied for reset and set operations, respectively (insets of Figure 3e). The pulse duration for the reset operation generally needs to be much longer than the time for the set operation, because the set process is mainly driven by the electric fields while the reset process involves thermally driven reactions; a reset operation therefore requires much more energy and time.[38] Successful pulse switching of the device was achieved until 50 cycles while maintaining a steady R_{on}/R_{off} ratio. Figure 3f shows the retention characteristics of the device at room temperature. The two resistance states of the device were maintained up to 10^4 s without apparent degradation. These memory characteristics confirm the improved fidelity of the NiO resistive memory by the incorporation of SiO_x-NDs.

In addition, RS properties of the BCP-modified resistive memory depending on the size of SiO_x-NDs and the morphology of SiO_x nanostructures were evaluated. As a comparison, 10 nm-diameter SiO_x-NDs and the 20 nm-width SiO_x lines were incorporated between NiO films and the top electrode (Pt/Ti), which was followed by the characterization of memory devices performance (Supporting Information, Figure S12). We already reported the formation of various silica nanostructures including sub-10 nm-scale spheres, cylinders, and perforated lamellae.[26] The best improvement of the uniformity and the repeatability were obtained in the case of the device with 20 nm-diameter SiO_x-NDs. This optimization may be achieved by the simultaneous attainment of enough insulating property and CF formation guiding capability. Although the uniformity improvement for the device with 10 nm-diameter SiO_x-NDs was slightly less than that for the device with 20 nm-diameter SiO_x-NDs, this result suggests that this technology can be applicable to ReRAM devices scaled down to 20 nm or further. Furthermore, it has been previously reported that 6 nm SiO_x-NDs can be formed by reducing the molecular weight of the PS-*b*-PDMS BCP.[39] In addition, to enhance the insulating effect, we can consider the use of vertical SiO_x cylinders with a high aspect ratio that can be formed using the same PS-*b*-PDMS BCP and a different assembly technique.[40] The device with 20 nm-width SiO_x lines showed the smallest uniformity improvement among them. This result implies that the filaments were less selectively grown because of the continuous edges of the SiO_x lines.

TEM Observations of Conductive Filaments. For verification of controlled CF formation *via* the SiO_x-NDs, we performed HRTEM and EDS analyses. Samples for TEM measurements were prepared with devices operated for more than 100 write cycles and cut by a focused ion beam (FIB). Figure 4 panels a–c and Figure 4 panels d–f show HRTEM images after the reset operation (HRS) and the set operation (LRS), respectively. First, at HRS, a cone-shaped nanostructure with a clearly different contrast from the background NiO was separated from the thin Ti layer, and its apex was oriented toward the sites without SiO_x-NDs (Figure 4a,b).

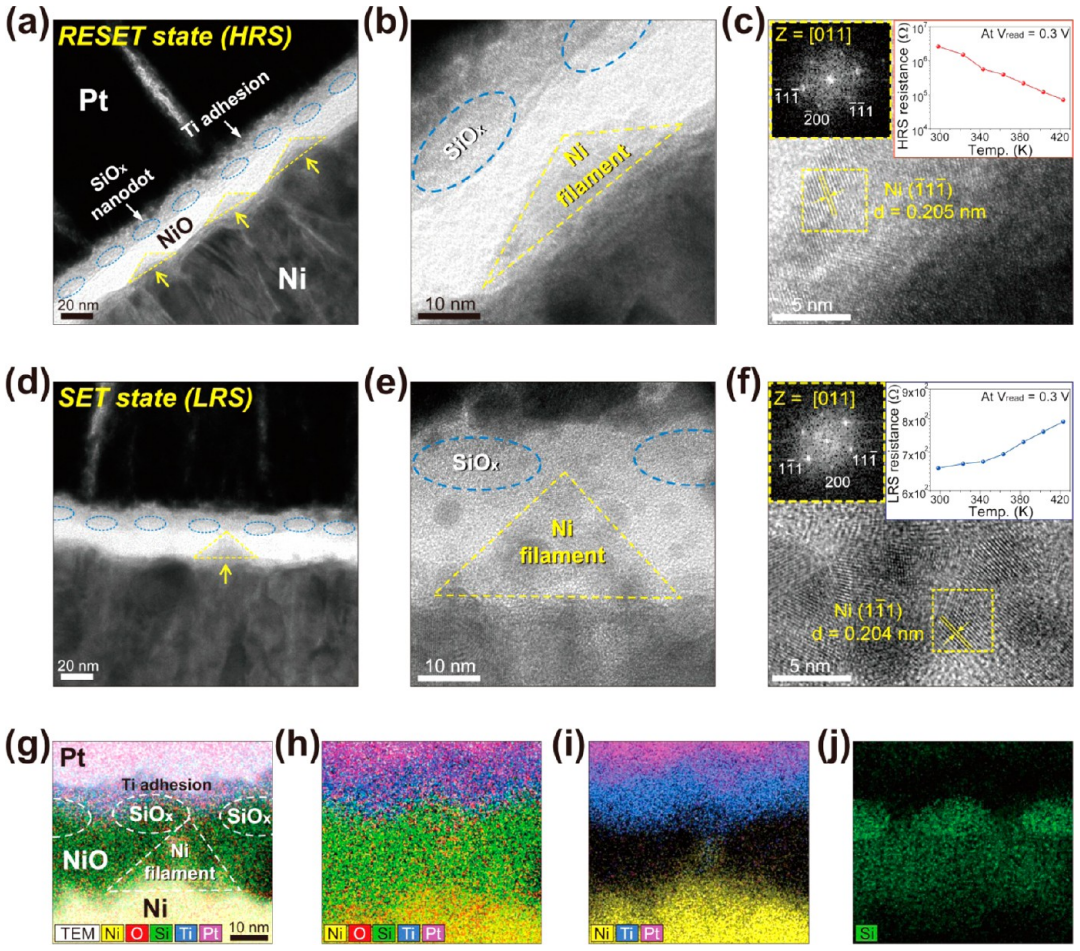

Figure 4. TEM and EDS mapping analyses for CFs observation in NiO memories with self-assembled SiO_x-NDs. TEM images of device (a−c) after the reset process (HRS) and (d−f) after the set process (LRS). The blue dotted circles represent the SiO_x-NDs, and the yellow dotted triangles indicate the Ni CFs. The inset images of c and f show fast Fourier transformed micrographs for the HRTEM images of Ni filaments, and the temperature dependence of the HRS/LRS resistance. EDS elemental mapping results (LRS) of (g) TEM, Ni, O, Si, Ti, and Pt, (h) Ni, O, Si, Ti, and Pt, (i) Ni, Ti, and Pt, and (j) Si.

Its high-magnification image also presented a polycrystalline structure, which is clearly distinguished from the amorphous NiO region (Figure 4c). The fast Fourier transform (FFT) pattern of the cone-shaped area shown in the inset of Figure 4c indicates that it is a face-centered cubic (FCC) structure along the [011] zone axis, and the *d*-spacing value along the [$\bar{1}1\bar{1}$] direction is 0.205 nm, which corresponds to the *d*-spacing of Ni.

Figure 4d and e show that the cone-shaped Ni filament at the LRS is directly connected to the Ti films, contrary to the HRS case, showing that the metallic Ni filaments act as current-conducting paths inside the NiO films. The vertex of the connected Ni filament is also oriented toward the region where SiO_x-NDs are not located, implying that the Ni cone observed for the HRS was modified from that in the LRS. The high-magnification image and the FFT pattern in Figure 4f show that the connected filament also has a Ni polycrystalline structure, corresponding to the filament nanostructure at the HRS. High-magnification HRTEM images are provided in Figure S14, showing the clear distinction between the amorphous NiO matrix and the Ni filament. In the EDS elemental mapping results in Figure 4g−i, the cone structure was found to have a Ni-rich stoichiometry, and was connected to TE (Pt/Ti). The Si elemental mapping image in Figure 4j indicates the sites of SiO_x-NDs; it is thus confirmed that the Ni filament was grown toward the sites without SiO_x-NDs as mentioned above. The TEM images in Figure 4 panels a and d show that the average width of Ni filaments contacting BE is about 29 nm, and the vertices have an average radius of curvature of 1−3 nm. Several research groups have previously reported that the lateral size of conductive filaments was about 15 to 40 nm,[4,10,11,20] which is comparable to that of our study. The size of conductive filaments are influenced by various parameters such as switching materials, cell size, device structure, thickness of active layer, compliance current during electroforming, and operating voltages.[9,41] We expect that the size of Ni CFs will be reduced when the above parameters are properly modified. For example, the voltage/current for electroforming would be smaller as the device size shrinks, resulting in the size reduction of CF. Additional

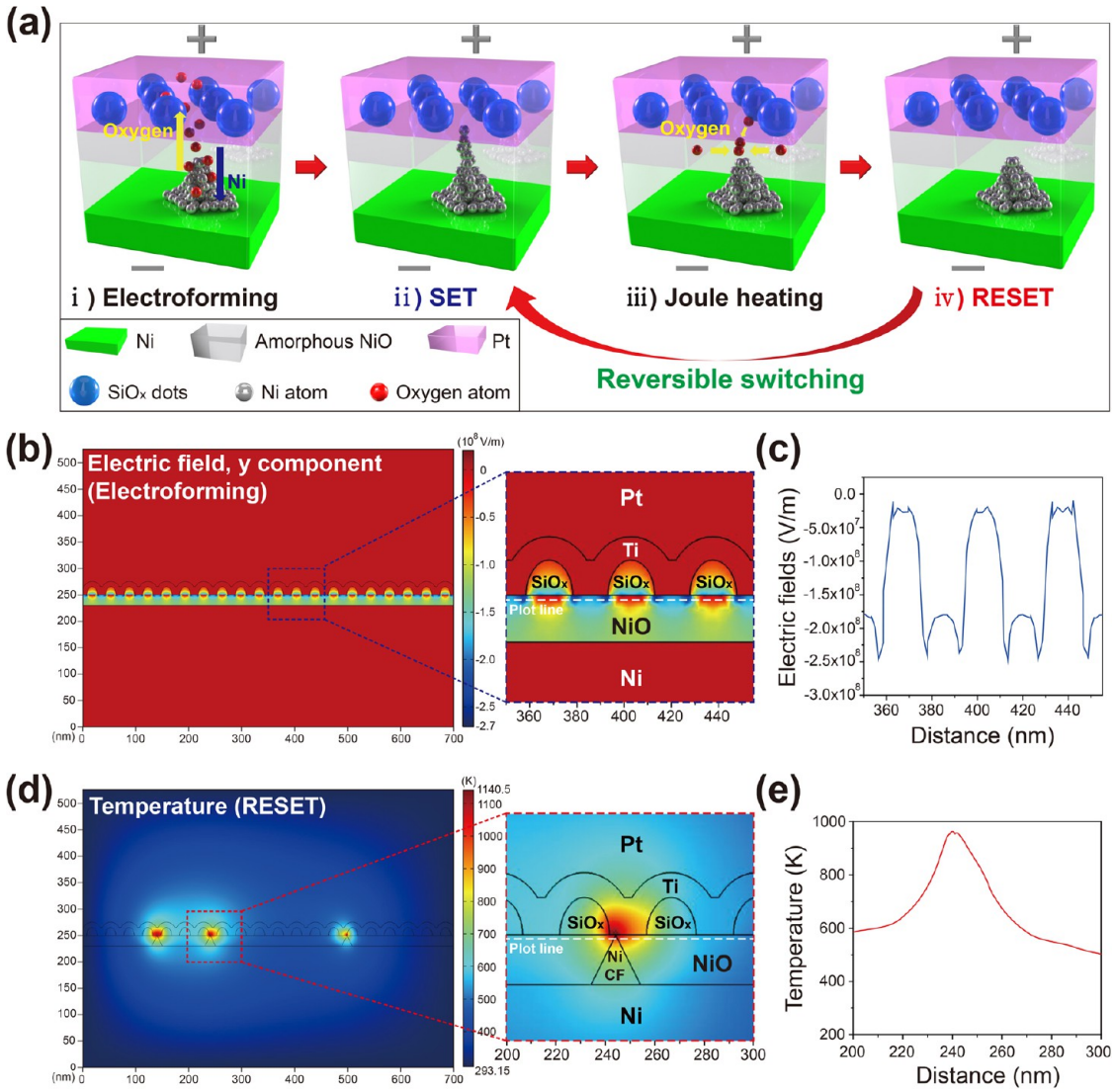

Figure 5. Operation mechanism and simulation results of NiO resistive memories with SiO_x-NDs. (a) Schematic diagrams of mechanism for electroforming and set/reset process of the device. The oxygen ions move toward the anode (corresponding to the opposite direction of oxygen vacancies), and the Ni ions in the NiO films migrate toward the cathode during the forming and set process. This results in the formation of a Ni filament in the area without SiO_x-NDs (LRS). Since Joule heating is generated by the thermochemical reaction during the reset process, the filament is ruptured and changed to NiO due to the migration of oxygen ions. Therefore, the resistive memory device is in a HRS. Electro-thermal simulations based on FEM of (b) the electroforming process and (d) the reset process in the cell with SiO_x-NDs. Profile graphs of (c) electric fields for the electroforming process and (e) temperature distributions for the reset process according to the distance at the interface between Ti films and NiO material.

TEM/EDS images collected from about 30 TEM specimens are presented in Supporting Information, Figures S15–S17 and provide consistent results supporting the formation of ruptured and connected Ni filaments after reset/set operations, respectively.

The temperature dependence of cell resistance is shown in the insets of Figure 4 panels c and f, providing further evidence of metallic filament formation. The resistance of the HRS sample decreased with temperature (inset of Figure 4c), indicating the insulating or semiconducting behavior of NiO. In contrast, the resistance of the LRS slightly increased with temperature (inset of Figure 4f), demonstrating that the low resistance of the NiO resistive memory is the result of the formation of metallic CF.[42] The linearity of the *I*–*V* curve replotted in log–log scale in the LRS also suggests a metallic-like Ohmic conduction mechanism (Figure S18 in the Supporting Information).[43] One notable point here is that, whereas many studies have previously reported that Ni filaments are grown along the grain boundary inside polycrystalline NiO,[34,35,37,44] cone-shaped Ni phase filaments are observed inside the amorphous NiO films without a grain boundary in the present study. The TEM and EDS analyses results suggest that the self-assembled SiO_x-NDs can control the formation/rupture of the metallic Ni filament in the amorphous NiO films, contributing to large uniformity improvement of unipolar NiO resistive memory.

RS Mechanism and Simulation Analyses. To illustrate the RS mechanism, schematic diagrams of a NiO memory device with embedded self-assembled SiO_x-NDs are shown in Figure 5a. First, under the high electric fields for the electroforming process, positively charged oxygen vacancies migrate toward the cathode (BE; Ni).[8,18,34,35] The negatively charged Ni vacancies in the NiO move toward the anode (TE; Pt/Ti).[45] These migrations of oxygen and nickel vacancies result in growth of the metallic Ni filament from the cathode (Ni) to the anode (Pt/Ti) (Supporting Information, Figure S16). The Ni filaments are mostly grown toward the regions without SiO_x-NDs, where the electric fields are concentrated. The oxygen effects into the SiO_x-NDs were negligible during the forming process since the insulating SiO_x-NDs modified only electric fields. Consequently, the Ni filament is directly connected to the anode as a current path (LRS). During the reset operation, high current density induces Joule heating at the end point of the filament, which causes oxygen diffusion from NiO or TE (Pt/Ti) to the filament.[8,18] Here, it was more favorable that the oxygen ions move into NiO or TE rather than the SiO_x-NDs moving to the filament, because the SiO_x-NDs do not have a direct contact with the CFs considering the TEM observation that the vertex of the connected Ni filament is oriented toward the region where SiO_x-NDs are not located. Moreover, SiO_x-NDs derived from the BCPs were found to be oxygen-deficient. As a result, the end point of a Ni filament is converted into NiO, and thus the filament is ultimately ruptured. When the set voltage is applied to the device again, the aforementioned migrations of oxygen and Ni vacancies will lead to the formation of the Ni filament; these behaviors are repeated for the reversible set/reset operations. Although oxygen vacancies are, in general, relatively more mobile than cations in transition metal oxides,[1] cations can also be mobile in some oxygen-rich transition metal oxides such as $Ni_{1-x}O$ and $Co_{1-x}O$, *etc.*[46] The oxygen-rich and Ni-deficient stoichiometry of the amorphous NiO films fabricated by RIE oxidation, which was revealed by EDS analysis result (Figure S4b in the Supporting Information), suggests the mobility of Ni vacancies. The local growth of metallic Ni filaments, which was experimentally confirmed from the TEM and EDS analysis results, is thought to be achieved when oxygen and nickel vacancies are sufficiently mobile in the $Ni_{1-x}O$ films.[44,47]

The BCP-modified NiO resistive memory device was simulated by using an electro-thermal model based on the finite element method (FEM) for further investigation of the *E*-field concentration effect and guided growth of filaments by the SiO_x-NDs. For the device with SiO_x-NDs, when the voltage for forming was applied to the TE, significantly modified electric fields distributions were obtained in the NiO films, and in particular high electric fields were concentrated on the regions without SiO_x-NDs, as shown in Figure 5b. It also should be noted that in the *E*-field profile graph presented in Figure 5c, the field was considerably enhanced at the edge region of SiO_x-NDs. These simulation results are consistent with the TEM analysis in Figure 4, where the Ni CFs were mainly grown toward the edge of the SiO_x-NDs, not the center of two SiO_x-NDs. In contrast, the electric field for the conventional device without SiO_x-NDs was uniformly distributed in the NiO films (Supporting Information, Figure S19a). From these results, the available locations of filament formation for the device employing the SiO_x-NDs were extremely limited compared to that for the conventional device, thus resulting in significant improvement in switching reproducibility and uniformity, as our experimental data show. Figure 5 panels d and e present the temperature distributions during the reset operation when the reset voltage is applied to the device and suggest that intense Joule heating occurs at the end point of Ni CFs.[48] The maximum temperature was calculated to be 1140.5 K, which is sufficient for the diffusion of oxygen vacancies into the NiO film or the TE for CF rupture.[5,19]

CONCLUSIONS

In summary, we introduced a novel, facile, and scalable approach that shows how the uniformity of RS parameters for unipolar NiO resistive memory devices can be significantly improved by employing a simple procedure based on BCP self-assembly technology. Self-assembled SiO_x-NDs were successfully formed between the electrode and the NiO active material, providing substantial reduction of operating voltage variations as well as HRS/LRS ratios. Growth and rupture of metallic Ni filaments in the amorphous NiO were directly observed through HRTEM and EDS analyses, demonstrating that the uniformly distributed SiO_x-NDs can guide RS operation by selective filament growth/rupture. Our simulation analyses confirmed that the use of SiO_x-NDs provided practical capability to modify the electric fields and temperature distributions in NiO memory. Considering the outstanding controllability, scalability, and large-area uniformity of BCP self-assembly, the findings of this study can provide a simple and practical solution to relieve the reliability issues in various filament-type resistive memories.

METHODS

Resistive Memory Devices Fabrication. Si samples with 150 nm-thick SiO_2 were prepared as substrates. Ni/Cr (250 nm/20 nm) were deposited by RF sputtering. NiO films (20 nm) were oxidized by using a RIE system (power = 200 W, press = 10 mTorr, O_2 flow = 10 sccm, time = 900 s). A Si-containing PS-*b*-PDMS

(20 nm SiO_x-NDs, MW = 56.1 kg/mol, f_{PDMS} = 17.1%; 10 nm SiO_x-NDs, MW = 28.0 kg/mol, f_{PDMS} = 11.5%; 20 nm SiO_x lines, MW = 45.5 kg/mol, f_{PDMS} = 33.5%) BCP was spin-coated on PS-OH (MW = 22 kg/mol) brush-coated NiO films. Samples were annealed under toluene vapor at room temperature, which resulted in the self-assembled PDMS in the PS matrix. CF_4 (21 s at 50 W) and O_2 (40 s at 60 W) plasma treatments followed so as to remove the PS layer and oxidize the PDMS dots. Finally, the TE (Pt/Ti) (250 nm/10 nm) was deposited by RF sputtering. The process of the reference samples was similarly performed except for the formation of self-assembled SiO_x-NDs.

Electrical Measurements. Electrical characterizations and evaluation were performed by using a Keithley 4200-SCS (DC voltage/current sweep), a Keithley 4225-PMU (pulse generator and waveform capture of voltage/current), and a 4225-RPM (remote amplifier/switches). The HRS/LRS of the devices were caculated at a read voltage of 0.3 V.

TEM/EDS Analyses. Samples for TEM observations were fabricated by using a dual beam FIB (FEI NOVA 200) and ion milling with Ar ions. HRTEM/EDS analyses were performed with a JEOL JEM-ARM 200F microscope (200 kV) and a BRUKER QUANTAX 400 EDS.

FEM Simulation. COMSOL multiphysics software (ALTSOFT) was used for the simulation modeling of the RS behavior in the memory device. The physical model was computed by an electrothermal method which was solved by the following equations for electric field and the temperature distribution by heat transfer. The electric field E in the device is given by

$$E = -\nabla V \tag{1}$$

where V is the electric potential. The mathematical model for heat transfer is the heat equation

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \Delta T) = Q \tag{2}$$

where ρ is the density, T is the temperature, C is the heat capacity, k is the thermal conductivity, t is the time, and Q is the heat flux. The heat generated by Joule heating Q is given by

$$Q = \frac{1}{\sigma}|J|^2 = \sigma|\nabla V|^2 \tag{3}$$

where σ is the electric conductivity and J is the electric current density. The electric field and temperature distribution were numerically extracted from the voltage defined on the TE surface, while the BE surface was selected as the ground.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Supplementary SEM/TEM images and EDS analysis, schematics of device fabrication, additional characteristic data, and theoretical study are included. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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